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CT and MRI image reconstruction based single-path delay feedback (SDF) FFT pipeline architecture

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ABSTRACT

Purpose: In radiology, several medical imaging modalities were used. In recent Biomedical systems, integrated circuits were used in the form of Application Specific Integrated Circuits (ASICs) to perform FFT. The raw data obtained from the acquiring equipment are reconstructed to image using Fast Fourier Transform (FFT). The contribution in the paper is to design an FFT integrated unit for converting the Magnetic Resonance (MR) signal into frequency spectrum of each phase encoding.
Materials and Methods: The image created is been transformed from the spatial projection using inverse Fourier transform. The k-space FFT information were back projected to obtain the MRI image. This paper presents an integrated circuit implementation of FFT processing elements used in Magnetic Resonance Imaging (MRI) reconstruction and ultrasonic imaging. The circuits designed in this work is to be used in the back-projection unit of MRI reconstruction. The complex periodic signal received from the receiver coils in MRI or piezoelectric disc in ultrasound and detector array in CT are analyzed using Fourier transform. The proposed single-path delay feedback (SDF) Decimation In Frequency (DIF) 4096-point FFT for image reconstruction was implemented in 65nm FPGA kit and programmed using VHDL in Quartus tool.
Results: This block becomes the part of the reconstruction unit of MRI image. The proposed design reduces the execution of instruction per cycle and the fixed point arithmetic provides low roundoff error.

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Conclusions: Since in MRI reconstruction the frequency encoding and phase encoding is combined to develop the images the proposed FFT will be useful. In Future application specific integrated circuits will be designed for the entire MRI back projection and reconstruction unit.

KEY WORDS

Keywords: FFT, CT, MRI, Image Reconstruction, Pipeline Architecture, FinFET, Adder

1. Introduction

In radiology, several medical imaging modalities like computed tomography, Magnetic resonance imaging and ultrasound were used for screening and diagnosis of various diseases. In the process, using various techniques data are recorded. The measured data is converted to image using the filtered back projection algorithm. The data represents the biologic metabolites of the region of interest. The composition of signals recorded from biological places were analyzed using the Fourier Transform. The raw data obtained from the acquiring equipment are reconstructed to image of human anatomy using Fast Fourier Transform (FFT). In recent Biomedical systems integrated circuits were used in the form of Application Specific Integrated Circuits (ASICs) to perform FFT and DWT [1]. The complex periodic signal received from the receiver coils in MRI or piezoelectric disc in ultrasound and detector array in CT are analyzed using Fourier transform. In MRI spectroscopy image is an example. Using convolution, the representation of different molecules in different frequencies are complex. Using FFT the number of multiplications and additions are reduced when compared to that used in the time domain. The radiology modalities Computed Tomography (CT), Magnetic Resonance Imaging (MRI), and Positron Emission Tomography (PET) use FFT and convolution for image analysis [2]. The inverse fast Fourier transform (IFFT) is an important image reconstruction method for k-space data with full Cartesian sampling. The FFT and IFFT play an important role in both phased array imaging and parallel imaging. Parallel imaging which uses multiple receive coils has additional blocks for Fourier transform blocks. So there is need for Integrated circuits which are faster and handle lot of raw data. In [3] a single-block memory-based FFT processor in FPGA was presented. The design has dual port memory for Radix 2 FFT design. Xia, Kaifeng et al [4] implemented memory-based fast Fourier transform (FFT) processors with a prime factor algorithm. High-radix–small-butterfly (HRSB) and a unified Winograd Fourier transform algorithm was implemented. In the paper [5] used the famous Vedic Multiplier (VM) and Carry Lookahead Adder (CLA) in FFT computation. For the implementation DRAM-VM-CLA architecture was followed in ASIC 180 nm technology. Ingemarsson et al [6] analyzed the pipeline single-path delay feedback (SDF) fast Fourier transform (FFT) architecture and implemented in Hardware. For implementation Xilinx Virtex-4 and Virtex-6 devices were used. The Algorithmic transformations was used in the implementation process. For Fourier-domain optical coherence tomography (FD-OCT), Tang Song-Nien et al [7] framed a multimode memory-based Fast Fourier Transform (FFT) processor. The design supports multiple-input multiple-output orthogonal frequency division multiplexing (MIMO-OFDM). The 4096-point FFTs can be able to access the data from sixteen memory paths. For implementation is done using the TSMC-0.18 µm CMOS technology core. The FPGA based OCT imaging consumes power in the range of few mWs. A low power Welch power spectral density (PSD) estimator to prevent multiplication in FFT was designed by AbdolVahab et al [8]. The reduction of multiplication was done using the combined coefficient selection and shift-and-add implementation (CCSSI) unit. Folded architectures were used for reduction of computational units involving multiplication. FPGA was used. By Ma Zhen-guo et al [9] a radix-2 decimation-in-frequency FFT algorithm was implemented using parallel butterfly architecture.

The work can be extended towards two-dimensional data. The 32 point architecture seems to be faster but less efficient when computational is concerned. Guo et al [10] designed a multi-FFT parallel architecture for 5G communication network. 16-parallelism butterfly were used and implemented for various radix schemes. The other features included are conflict-free memory access and a system-on-chip (SoC) architecture was used. Garrido, Mario et al [11] reduced the use of distributed logic by utilizing a novel 4096-point radix-4 memory-based fast Fourier transform (FFT). The implemented field programmable gate array conflict-free. Wang et al [12] designed a conflict-free data-access scheme FFT module which has RAMs with single port. The area is reduced by using this architecture. The speed is improved using input/output (I/O) data parallelism. The field-programmable gate array is done TSMIC 40-nm CMOS technology. Liu, Shaohan and Dake Liu [13] used a design a FFT processor for 4G and 5G. The 4096-point FFT is simulated at 65nm. The mixed radix design is a 16-bit data Memory-based architecture. Thakur et al [14] used Parallel prefix (PP) adder to implement FFT. The designed radix -2 FFT is implemented with Parallel prefix (PP) adder, and Wallace multiplier using Brent Kung PP adder (M2P2). In another design Landner Fischer PP adder (M3P3) and Han Carlson PP adder (M4P4) were used [15]. Overlap between input data caching is done using a method named "in-place data caching". Four memory banks were employed. Single-port and four banks working in parallelism is done. A communator consisting of multipath and pipelining structure was presented [16]. The algorithm is a radix-2-time decimation algorithm. The speed is increased by pipelining and register counts are optimized.

In literature, several methods are used for image reconstruction which converts the acquired K- space data to real images in spatial domain [17,18]. Some of the methods are Artificial neural network, Radon Transform, DFT, and Parametric technique. In parametric methods like Moving Average (MA) data extrapolation is used, The Autoregressive (AR) and Autoregressive Moving average (ARMA) uses the extrapolation of raw data. Sparse Fast Fourier Transform (SFFT) proposes achieving million-point FFT per second with a constraint of maximum 500 non-zero frequency coefficients. Its architecture includes the Radix22 single-path delay feedback (SDF) decimation in frequency (DIF) 4096-point FFT with maximum operating frequency in 121.2MHz. There are other studies to reduce the circuit complexity with algorithms to minimize the size and power of the FFT processor using coefficient memory reduction and switching activity analysis schemes.

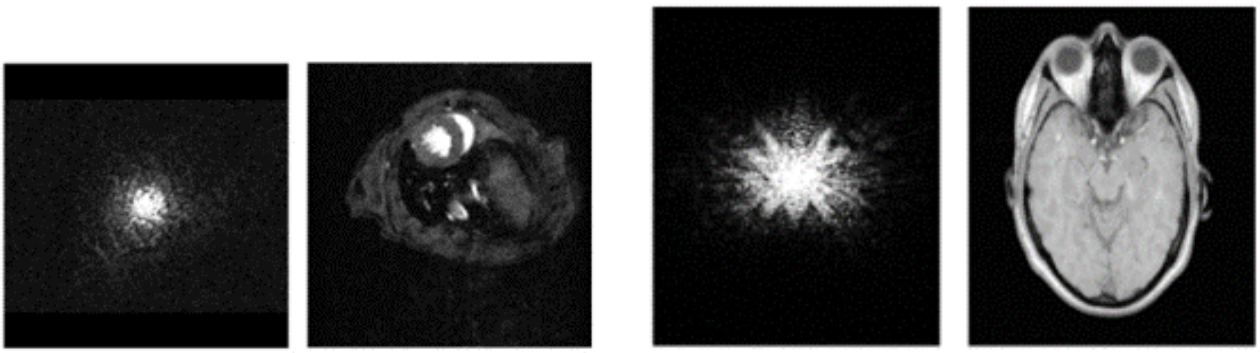
Radix-2 decimation-in-time 16-point FFT architecture uses the multiplier and adders. The structures based on distributed arithmetic includes blocks like (a) complex multiplication by twiddle factors, (b) butterfly computation with bit-parallel add- sub units, and butterfly computation with shared add/sub unit. In (a) and (b), all In (a) and (b), all the signals are real-valued and, signals are complex-valued. The last block is the P/S: Parallel-to-serial converter. The analog units in the reconstruction unit uses operational amplifiers which are low power. In recent times multigate devices were used to minimize power [19]. The FFT units were part of different applications including 5G communication system [20].

The purpose of the work or study is to investigate the integrated circuit implementation of FFT processing elements used in CT, Magnetic Resonance Imaging (MRI) reconstruction and ultrasonic imaging. The need of image reconstruction systems, efficient buffering and pipelining is addressed in this work. The study presents the various methods used for the reconstruction and a proposed method based on single-path delay feedback (SDF) decimation in frequency (DIF) 4096-point FFT is presented. The hardware design in FPGA is implemented in different CMOS technology like 65nm and 90nm. The comparison of methods was made.

2. Materials and methods

Radiology and Fast Fourier Transform (FFT)

The data obtained from the equipment is converted into image using FFT for CT, MRI, and ultrasonic imaging. The human anatomy can be reconstructed. Here in the process the data is filtered first and FFT is applied to the data. An example reconstructed data from original MRI raw data is shown in figure 1.a (raw data) and its reconstructed data. The beating heart of the mouse is depicted. The actual acquisition rate is 127Hz. The human head is shown in figure 1.b. The reconstruction was done with 16 axial slices. All these images used 256x256 arrays.



a) b)

Figure 1 *a) raw data and reconstructed data. b) human head and its reconstruction*
Here the raw data of MRI is analyzed using Fourier space called k-space. IFFT is performed with the k-space to obtain reconstructed image. In image reconstruction block FFT and convolution are heavily used in these modalities. The algorithm for image reconstruction could be different and specific to the device manufacturers but each of them usually uses FFT and convolution.

CT Image Reconstruction Process

During CT data acquisition X-rays from a source pass through a body to a detector to obtain one view. The remaining views are obtained by rotating the source and detector inside the CT gantry in specific radial increments, until a complete 360-degree rotation is completed to obtain one image slice comprised of those views. Each sample in a view is the summation of all values along the ray that points to that sample. In Fourier reconstruction, first a 1D FFT is taken of each view, therefore requiring approximately 700 1D FFTs for a 512x512 image slice. Secondly, these frequency domain view spectra are then used to calculate the 2D frequency spectrum of the image using convolution and Fourier slice theorem, requiring ~700 convolutions. Thirdly, an inverse FFT is taken of the spectrum to obtain the reconstructed image in the time domain using filtered back-projection technique, which requires an additional ~700 FFTs. By rough approximation this requires a total of about 1400 FFTs and 700 convolutions (excluding the convolution in filtered back-projection to be conservative) per 512x512 image slice.

A CT machine can produce 64, 128, 256 slices, and the number of slices needed for a study will completely depend on the physician. Using a 64-slice CT machine, producing a 512x512 image or slice, with each slice on average having 700 views, then based on the explanation above, the total number of FFTs would be approximately 89000 (64*1400) and the convolutions count would be approximately, 44800 (64*700). A larger study like CT angiography and cardiac CT will have a much higher number of views even for the same CT slices machine, hence a higher number of FFTs and convolution would be needed in those views. For small data sizes, the brute force method can be optimal, however as datasets get larger, the FFT method is faster. The output from either method is the same and users can choose to deploy the method they like.

Method 1: Brute Force Convolution

The “brute force” algorithm computes the convolution using the definition of convolution and not the fast Fourier transform. It drags the filter matrix over the image. At every pixel on the image, the values of the filter are multiplied by the corresponding values of the image that the filter is over. The products are summed, and this sum becomes the value of the pixel on the output image.

Proposed On-Chip Methodology of Image Reconstruction

For image reconstruction systems, efficient buffering and pipelining is necessary. The proposed method is based on single-path delay feedback (SDF) decimation in frequency (DIF) 4096-point FFT. The hardware design can be of ASIC or FPGA type. FFT hardware implementation uses more area and processing elements. Since in our work more slices are taken the architecture is larger. The architecture contains elements as shown in figure.2. The FPGA based image reconstruction uses the

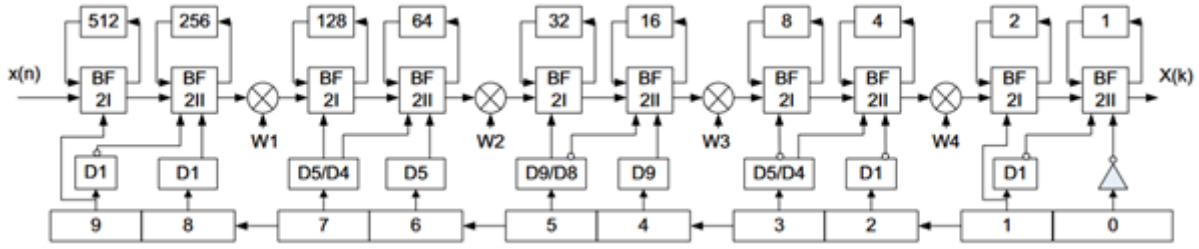


Figure.2. *N-point radix-22 SDF pipeline FFT core*

Table 1 Different Blocks in the FFT based Architecture	
	VLSI Blocks Used In This Work
Twiddle Factor Storage Block	Memory Device
SDF-BF	Multiplexer, Adder, Subtractor, Buffer
Trivial Multiplier	Multiplexer, AND gate, buffer, Inverter
N-point radix-22 SDF pipeline FFT core	SDF BF units, Multiplier Control unit Clock unit

Table.2 Parameter analysis of SDF BF		
CMOS Technology	65nm	
FPGA Device Used	EP3C5F256C6	
LUT	Available	5136
	Used	4
	utilization	< 1
Power (mW)	Core Dynamic Power Dissipation	0.57
	Core Static Power Dissipation	46.13
	I/O Thermal Power Dissipation	21.69
	Total Thermal Power Dissipation	68.38
Delay (nS)	7.739	

Circuit proposed with single-path delay feedback architecture. The implementation was done in EP3C5F256C6 Altera kit. In the FPGA the twiddle factors and data are stored in the memory. The speed is optimized using pipeline. The architecture shown in Fig.2 uses log4 N -1 complex multipliers and 4 log4 N adders. The limitation in frequency can also be avoided. The scaling of 'W' is done with Fixed-point arithmetic operation. This minimizes the round-off error. Simple control logics are used in the architecture with N -1 data size. The pipelining reduces the instruction per clock cycle. The look-uptable consisting of the twiddle factors. Matlab is used to calculate the twiddle factor.

In MRI, the signals observed by the radio frequency (RF) coils are analyzed and converted using high-speed analog-to-digital converter.

The proposed FFT design and convolution based design has components and memory to store the intermediate data The different blocks of the architecture is shown in table 1. The buffer design is an important part of the FFT architecture. The buffers used in the FFT architecture are of three different types. Input buffer, output buffer and delay buffer. When input buffer takes the input to the FFT block, the output buffer used to drive stages or fanouts. The delay buffer forms the part of the processing unit of the FFT. Design of clock and flops/

1. Trivial multiplier Implementation

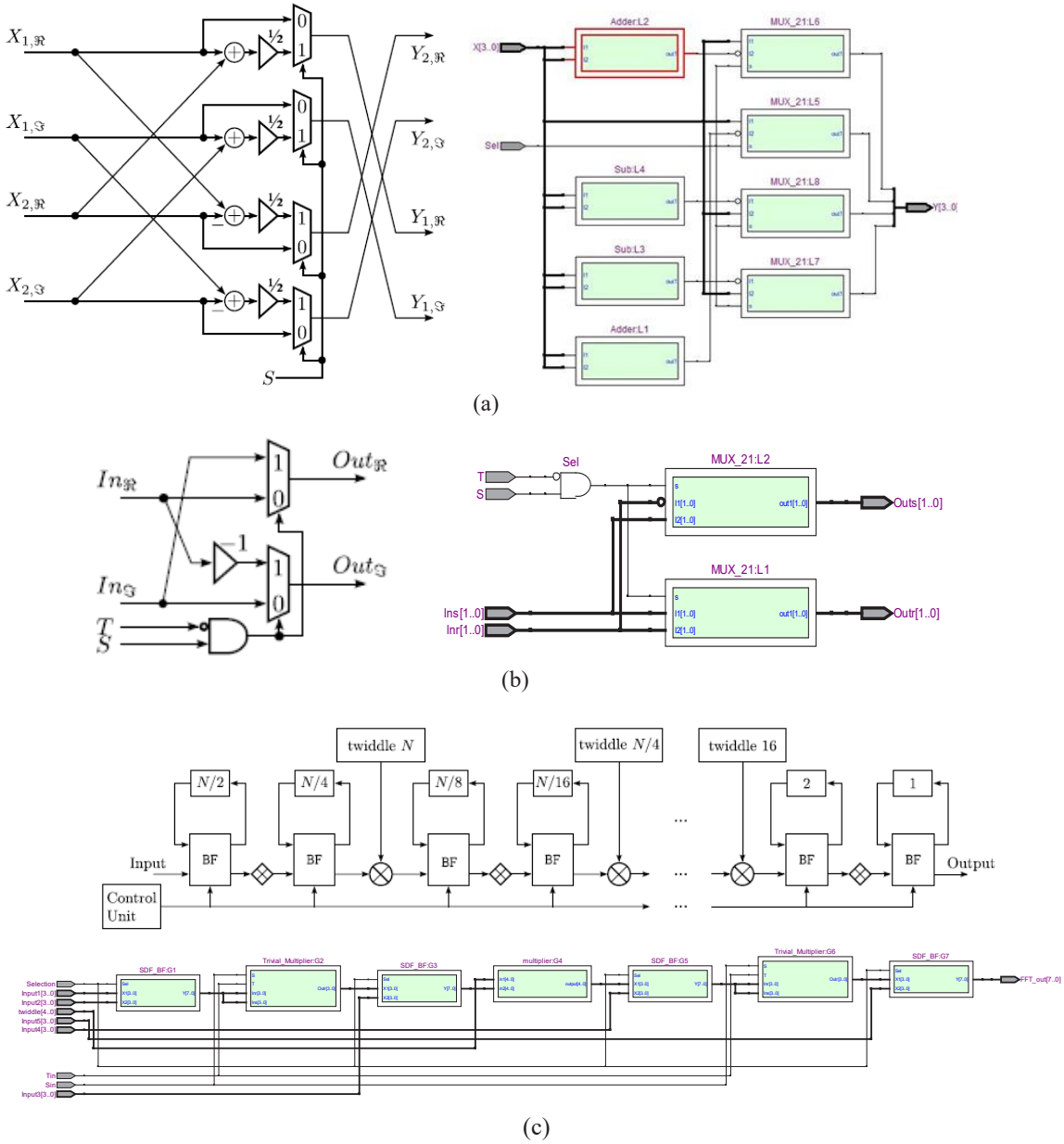


Figure 3 *The Circuit and RTL view of (a) SDF-BF (b) Trivial Multiplier (c) N-point radix-22 SDF pipeline FFT core*

latch influences more in terms of the power and the performance of the circuit.

The motive of the clock is to tie up the signals with time. The clocks are not needed for some problems. There may be a problem arises to minimize the overhead caused due to the usage of clocks and it also causes clock skew ad latch/flop overheads. To holding state the clock works with flop/latch. Latch tends to store data when the clock is low and flip flop stores the data when the clock rises. Clock is not needed when the delay is same for every path and the stage is stored in the gates and the wires. The signals stay is corresponding to time is known as wave pipelining. This may not be done as practical, so the values of signal are kept in the system.

Table 3. Parameter analysis of Trivial Multiplier		
CMOS Technology	65nm	
FPGA Device Used	EP3C5F256C6	
LUT	Available	5136
	Used	4
	utilization	< 1
Power (mW)	Core Dynamic Power Dissipation	0.68
	Core Static Power Dissipation	46.13
	I/O Thermal Power Dissipation	22.22
	Total Thermal Power Dissipation	69.03
Delay (nS)	8.162	

2. 16-point radix-2^2 SDF pipeline FFT core Implementation

Table 4. Parameter analysis of 16-point radix-22 SDF pipeline FFT core		
CMOS Technology	65nm	
FPGA Device Used	EP3C5F256C6	
LUT	Available	5136
	Used	36
	utilization	< 1
Power (mW)	Core Dynamic Power Dissipation	1.30
	Core Static Power Dissipation	46.13
	I/O Thermal Power Dissipation	19.17
	Total Thermal Power Dissipation	66.60
Delay (nS)	14.254	

Table 5. Parameter analysis of FFT developed in different nm technologies

Technology	Device	LUT			Power Dissipation (mW)				Delay (nS)
		Available	Used	Utilization (%)	Core Dynamic Power Dissipation	Core Static Power Dissipation	I/O Thermal Power Dissipation	Total Thermal Power Dissipation	
90nm-existing Conventional FFT	EP2S15F484C3	12480	6	<1	3.74	303.40	57.78	364.92	9.749
65nm-Existing Conventional FFT	EP3S-L50F484C2	38000	6	<1	3.21	370.45	51.49	425.15	10.184
65nm Proposed method	EP3C5F256C6	5136	6	<1	1.30	46.13	19.17	66.60	14.254

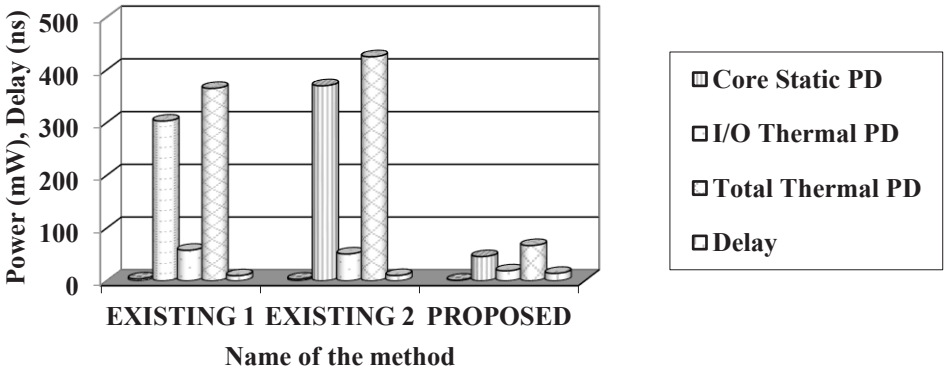


Figure 4. *Parameter comparison of FFT implemented in various methods.*

Each signal should be the successor to the predecessor so that it will be easy for fast operation. With the back-to-back of two latches the flip flop is built but the delay of clocks may slow down the path. There are two issues in the clock distribution. They are latch/flip flop delay and clock skew. In latch/flip flop delay, there is an approximate delay of 1.5 FO4. Two latches per cycle is greater than 15% of a cycle. The clock skew is constant in pc is harder where the cycle times are falling. So the experiments in engineering should grow with the clocks. If generating the clock gets harder than the radical approach has been used to eliminate it together. Local information can be used. Sequencing the information which is bundled with signals are called self-timed design.

General idea:

Instead of using clocks local information can be used to sequence the data. The readiness of the input values and state of next stage logic can sequence the pipelined logic. By using this local information there are some benefits can be obtained such as co clock or clock skew can be occur and circuits can run in their own speed. But some new problems are found. Decisions can be made in accordance with local information. This leads to take high time, area, power and delay while sending the decisions to the logic gates. To hide the delay, delay matching technique has been used. This may cause status quo to be present for a while. To reducing the skew on clock distribution the following should be concentrated. By reducing the skew the wire delay and the buffer delay also reduces. But to the required levels the delay cannot be reduced. The delay can be kept small in order to balance the delay in each path. This may escape from total delay problem and stick in matching problem. And T should be smaller than Tdrive. The technique clock trees is used reduce the skew. The selected delay should match the different branches of the tree. If the buffer delay and wire delay matches the skew will be zero.

3. Results and discussion

the proposed methods show the benefits of clock skew avoidance which finds useful in k-space analysis. The frequency encoding and phase encoding during the reconstruction process require circuits which should be free from skew and should run at high speeds. Delay matching technique is included in the proposed design to reduce wire delay and the buffer delay. The proposed single-path delay feedback (SDF) decimation in frequency (DIF) design was implemented in Quarter II. Figure. 3(a) shows the circuit and the RTL view of the SDF BF circuit. The circuit consists of the adder, multiplier and multiplexer as the major components. The circuit SDF BF, Trivial Multiplier and 16-point radix-22 SDF pipeline FFT core were implemented and the performance is presented. The design has been tested on Cyclone IV hardware development kit. Figure 3(b) shows the circuit and RTL of Trivial Multiplier. Figure 3(c) shows the circuit and RTL of 16-point radix-22 SDF pipeline FFT core. Table.2, 3 and 4 contains the Parameter analysis of SDF BF, Trivial Multiplier and 16-point radix-22 SDF pipeline FFT core.

The FFT architecture implemented in the different

technology device is shown in table.5. Comparative Graph shows the variation of power and delay of various FFT architecture. The conventional direct form FFT is compared with the proposed design. From the table it can be observed that the 90nm technology consumes more power but nominal delay. This parameter is taken into consideration for the integrated circuit. The comparative graph of the methods is shown in figure.4. Since most integrated circuits require low power supply, the power consumption becomes a determining factor. Since large computation is to be done the proposed design has more delay when compared to higher technology like 90nm. This is the disadvantages but when power is considered the advantage of the method is more.

4. Conclusion

The FPGA implementation of the FFT architecture for image reconstruction block is presented. The circuit provides low power consumption for MRI, CT and US units. The proposed single-path delay feedback (SDF) decimation in frequency (DIF) design was implemented in Quarter II and Cyclone IV hardware development kit. The processing elements like adder, multiplier and multiplexer were implemented for the design of proposed method. From the results it's been observed that the method proposed in this paper is advantages in area and power. The power consumption in the integrated circuit is minimized. While the method provides better delay but comparatively high when compared to the existing methods. The FFT blocks implemented in reconfigurable devices with less roundoff error and is suitable even if the k-space increases. In future, the work will be expanded to implement filters for removal of anatomical motion artifacts which affects the MRI scanning process. In addition, the FPGA based device will be implemented in application specific integrated circuits. **R**

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